In the Specification:

On page 1, lines 6-17, please delete:

"The below listed applications, as indicated by serial number and filing date, are all assigned to the assignee of the instant application and are co-pending and related to the instant application:

Serial No.	Filing Date
08/370,761	12/23/94
08/386,894	02/10/95
08/386,563	02/10/95
08/457,650	06/01/95
08/457,651	06/01/95
08/497,354	06/30/95
08/505,576	07/20/95
08/553,156	11/07/95
08/506,438	07/24/95

as well as a U.S. patent application entitled, 'Burst EDO Memory Device,' filed April 11, 1996",

and insert therefor:

The below listed applications, as indicated by serial number and filing date, are all assigned to the assignee of the instant application and were or are co-pending with and related to the instant application: Serial No. 08/370,761, filed December 23, 1994 (now U.S. Patent 5,526,320, issued June 11, 1996); Serial No. 08/386,894, filed February 10, 1995 (now U.S. Patent 5,610,864, issued March 11, 1997); Serial No. 08/386,563, filed February 10, 1995 (now U.S. Patent 5,652,724, issued July 29, 1997); Serial No. 08/457,650, filed June 1, 1995 (pending); Serial No. 08/457,651, filed June 1, 1995 (now U.S. Patent 5,675,549, issued October 7, 1997); Serial No. 08/497,354, filed June 30, 1995 (now U.S. Patent 5,598,376, issued January 28, 1997); Serial No. 08/505,576, filed July 20, 1995 (now abandoned); Serial No. 08/553,156, filed November 7, 1995 (now U.S. Patent 5,721,859, issued February 24, 1998); Serial No. 08/506,438, filed July 24, 1995 (now U.S. Patent 5,729,503, issued March 17, 1998); and Serial No. 08/630,279, filed April 11, 1996 (now U.S. Patent 5,661,695, issued August 26, 1997).

In the Claims:

Please amend Claim 22, 23 and 32 as indicated.

22. (Amended) A memory circuit, comprising:

control logic for providing a selected mode control signal;

selection and temporary storage circuitry for receiving and storing a first external address; and

a multiplexer coupled to the selection and temporary storage circuitry and to the control logic for receiving the first external address and the selected mode control signal respectively therefrom and for switching the memory circuit between a burst mode and a pipelined mode.